CHAPTER 5. CIRCUIT DESCRIPTION

[1] Circuit description

1. General description

In this machine, the facsimile control block except the printer control is mainly composed of the units shown in Fig. 1.

2. PWB configuration

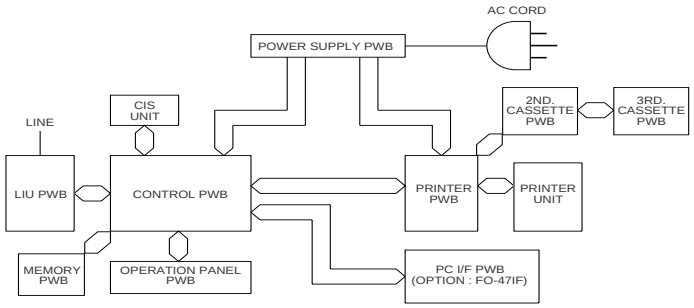


Fig. 1

1) Control PWB

The control PWB controls all the other operations except the printing operation of the printer.

2) LIU PWB

The LIU PWB controls the I/F telephone function of the circuit with the control signals from the control PWB.

3) CIS UNIT

CIS UNIT converts the image of the sending or copying draft into the photoelectric signals and transmits the signals to the control PWB.

4) Operation panel PWB

The operation panel PWB detects the key input, turns on and off LED and displays LCD according to the control signals from the control PWB.

5) Power supply PWB

DC voltages (+5V, +24V) are produced from AC120V, and are supplied to the printer unit and control PWB unit.

6) PC I/F PWB (Option : FO-47IF)

An interface to PC is done by IEEE1284, and image data (bitmap) from PC are outputted to the printer.

7) Memory PWB

The 2MByte image memory composed by flash memory which can be supported. When FO-3MK (OPTION) installed, a capacity rise is possible to 5 MByte.

8) 2nd. cassette PWB

The paper feeding control is relayed from the 2nd. cassette.

9) 3rd. cassette PWB

The paper feeding control from the 3rd. cassette is relayed and the feeding motor is driven.

[2] Circuit description of control PWB

1. General description

The control PWB is composed of the following blocks.

① Main control block
② Image memory block
③ Modem block
④ Image signal process block
⑤ Speaker amplifier
⑥ Reading process and mechanical control block
⑦ Gate array (A) block
⑧ Gate array (B) block
⑨ CODEC block
⑩ Page memory block
⑪ Drive block
⑫ JBIG block

2. Description of each block

(1) Main control block

The main control block uses RISC microprocessor HD6437021 as CPU, being composed of ROM (2 MByte), DRAM (2 MByte) and SRAM (256 KByte).

1) SH7021 (IC27): pin-100, QFP (main CPU)

The device is a microprocessor which integrates the peripheral functions, using CPU of 32-bit RISC type as the core. In the instrument, the following peripheral functions are mainly used.

① ROM of 32 KByte and RAM of 1 KByte are integrated.
A part of programs are stored in the integrated ROM.
② DMA controller (4 channels are provided, and 2 channels alone are used.)
ch.0: Used to transmit image data between CODEC (HD813201F) and DRAM (IC16).
ch.2: Used to transmit image data between Flash memory (option) and DRAM(IC16).
③ Clock-synchronous type serial communication interface commands and statuses are communicated with PCU.
④ Interruption
$\overline{IRQ4}$, $\overline{IRQ7}$: Interruption request from gate array (A) (LZ9FJ59)
$\overline{IRQ6}$: Interruption request from gate array (B) (LR38292)
$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQ3}$, $\overline{IRQ5}$, $\overline{IRQ7}$: Not used.
$\overline{NMI}$: Not used.
⑤ DRAM controller
Addressing to DRAM(IC16) of the system and control and refresh control of $\overline{RAS}$ and $\overline{CAS}$ signals are executed.
⑥ Timer and watch dog timer
⑦ General-purpose I/O port
Control of Liu and control of analog process of read signals are executed.
⑧ Clock oscillation
Crystal oscillator of 19.66 MHz is connected for operation of 19.66 MHz.
⑨ Generation of alarm sound and ringer sound
The keys on the operation panel are pressed to respectively generate the key input sound, alarm sound and ringer sound.

2) 27C160 (IC4): pin-42, DIP (EPROM)

Programs are stored in a 16 Mbit ROM.

3) HY5118164 or MSM5118165 (IC16): pin-42, SOJ (DRAM)

Used as the system memory of main CPU and transmission buffer of communication.

4) SM8578BV (IC30): pin-8, SOP (Real time clock IC)

It is oscillated with the quartz oscillator of 32.768 kHz, and the clock and calendar functions are provided. Even if the power supply of the main body is turned off, it is backed up with lithium battery. This device executes the clock-synchronous type serial communication with the gate array (A), and CPU can know the time and date through the gate array (A).

SH7021 (IC27) Terminal descriptions

Classification	Code	Terminal No. (TFP-100B)	I/O	Name	Function
Power	Vcc	13, 38, 63, 73, 80, 88	I	Power	Connect to the power supply. Connect Vcc terminals to the power units of all systems. If any open terminal is present, it will not operate
	Vss	4,15,24,32, 41,50,59,70, 81,82, 92	I	Ground	Connect to the ground. Connect Vcc terminals to the power units of all systems. If any open terminal is present, it will not operate.
Clock	EXTAL	71	I	External clock	Connect to the quartz oscillator. Moreover, EXTAL terminal can input the external clock. Use the same frequency for the quartz oscillator, external clock and system clock.
	XTAL	72	I	Crystal	Connect the quartz oscillator. Connect the same frequency of the system clock (CK). To input external clock from EXTAL terminal, open EXTAL terminal.
	CK	69	O	System clock	Supply system clock to the peripheral device.
System control	$\overline{\text{RES}}$	76	I	Reset	If this terminal is turned to the low level when NMI is at the high level, it will be brought into the power-on state. If this terminal is turned to the low level when NMI is at the low level, it will be brought into the manual reset state.
	$\overline{\text{WDTOVF}}$	75	O	Watch dog timer overflow	It is overflow output signal from WDT.
	$\overline{\text{BREQ}}$	60	I	Bus right request	Select the low level to make the external device request the release of bus right.
	$\overline{\text{BACK}}$	58	O	Bus right request acknowledge	It indicates that the bus right is released to the external device. When receiving $\overline{\text{BACK}}$ signal, the device which outputs $\overline{\text{BREQ}}$ signal can know that bus right is obtained.
Operation mode control	MD2~ MD0	79~77	I	Mode setting	The terminal determines the operation mode. During operation, don't vary any input value. The relationship between MD2 thru MD0 and operation modes are shown in the following list.
Interrupt	NMI	74	I	No-maskable interrupt	This is the interrupt request terminal which can not be masked. Either leading edge or trailing edge is selected for receiving.
	$\overline{\text{IRQ0}}$~ $\overline{\text{IRQ7}}$	65,66,67,68, 97,98,99,100	I	Interrupt request 0 thru 7	This is the interrupt request terminal which can be masked. Either level input or edge input can be selected.
	$\overline{\text{IRQOUT}}$	61	O	Interrupt request output in the slave mode	It indicates that a factor of interrupt occurs. It indicates that interrupt occurs in the bus release mode.
Address	A21~A0	45~42,40,39, 37~33,31~25, 23~20	O	Address	Address is output.
Data bus	AD15~ AD0	19~16,14, 12~5,3~1	I/O	Data bus	Bidirectional data bus of 16 bits Multiplex is possible with the low-order 16 bits of the address.
	DPH	64	I/O	High-order side data bus parity	Parity data corresponds to D15 thru D8.
	DPL	62	I/O	Low-order side data bus parity	Parity data corresponds to D7 thru D0.

(Continuing)

Relationship between MD2 thru MD0 and operation modes

MD2	MD1	MD0	Operation mode	Integrated ROM	Bus width of area 0
0	0	0	MCU mode	Invalid	8-bit size
0	0	1			16-bit size
0	1	0		Valid	—
0	1	1	(Reserved)	—	—
1	0	0	(Reserved)	—	—
1	0	1	(Reserved)	—	—
1	1	0	(Reserved)	—	—
1	1	1	(Reserved)	—	—

SH7021 (IC27) Terminal descriptions

Classification	Code	Terminal No. (TFP-100B)	I/O	Name	Function
Bus control	$\overline{WAIT}$	54	I	Wait	It is input to insert Tw into the bus cycle during access to the external space.
	$\overline{RAS}$	52	O	Low address strobe	Timing signal of low address strobe of DRAM
	$\overline{CASH}$	47	O	High-order column address strobe	Timing signal of column address strobe of DRAM It is output for access to high-order 8 bits of data.
	$\overline{CASL}$	49	O	Low-order column address strobe	Timing signal of column address strobe of DRAM It is output for access to low-order 8 bits of data.
	$\overline{RD}$	57	O	Read	It indicates that outside is read out.
	$\overline{WRH}$	56	O	High-order write	It indicates writing at the external high-order 8 bits.
	$\overline{WRL}$	55	O	Low-order write	It indicates writing at the external low-order 8 bits.
	$\overline{CS0}$~$\overline{CS7}$	46~49, 51~54	O	Chip select 0 thru 7	Chip select signal for external memory or device
	$\overline{AH}$	61	O	Address hold	Address hold timing signal for device which uses multiplex bus of address/data
	$\overline{HBS}$, $\overline{LBS}$	20 56	O	Low-/high-order byte strobe	Strobe signal of high/low byte (Commonly used with AO, $\overline{WRH}$.)
	$\overline{WR}$	55	O	Write	Output during writing. (Commonly used with $\overline{WRL}$.)
DMAC	$\overline{DREQ0}$, $\overline{DREQ1}$	66,68	I	DMA transfer request (Channels 0 and 1)	Input terminal of DMA transfer request from external
	DACK0, DACK1	65,67	O	DMA transfer request receiving (Channels 0 and 1)	It indicates that DMA transfer request is received.
16-bit integrated timer pulse unit (ITU)	TIOCA0, TIOCB0	51, 53	I/O	ITU input capture/output conveyor (Channel 0)	Output terminal of input capture input/output conveyor
	TIOCA1, TIOCB1	62, 64	I/O	ITU input capture/output conveyor (Channel 1)	Output terminal of input capture input/output conveyor
	TIOCA2, TIOCB2	83, 84	I/O	ITU input capture/output conveyor (Channel 2)	Output terminal of input capture input/output conveyor
	TIOCA3, TIOCB3	85, 86	I/O	ITU input capture/output conveyor (Channel 3)	Output terminal of input capture input/output conveyor
	TIOCA4, TIOCB4	87, 89	I/O	ITU input capture/output conveyor (Channel 4)	Output terminal of input capture input/output conveyor
	TOCXA4, TOCXB4	90, 91	O	ITU output conveyor (Channel 4)	Output terminal of output conveyor
	TCLKA~ TCLKD	65,66,90, 91	I	ITU timer clock input	External clock input terminal to counter of ITU
Timing pattern controller (TPC)	TP15~ TP0	100~93, 91~89, 87~83	O	Timing pattern Output 15 thru 0	Output terminal of timing pattern
Serial communication interface (SCI)	TxD0, TxD1	94, 96	O	Sending data (Channels 0 and 1	Sending data output terminal of SCI0, 1
	RxD0, RxD1	93, 95	I	Receiving data (Channels 0 and 1)	Receiving data input terminal of SCI0, 1
	SCK0, SCK1	97, 98	I/O	Serial clock (Channels 0 and 1)	Clock input/output terminal of SCI0, 1
I/O port	PA15~ PA0	68~64, 62~60, 58~51	I/O	Port A	Input/output terminal of 16 bits Input/output can be assigned for each bit.
	PB15~ PB0	100~93, 91~89, 87~83	I/O	Port B	Input/output terminal of 16 bits Input/output can be assigned for each bit.

(2) Image memory block

This block is composed of memory PWB circuit.
Refer to [2-1] Circuit description of memory PWB for the details.

(3) Modem block

The block is mainly composed of the modem R288F (IC41), and is provided with the following modem function.

Table 1-1. Configurations, Signaling Rates, and Data Rates

Configuration	Modulation 1	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Symbol Rate (Symbols/Sec.)	Bits/Symbol - Data	Bits/Symbol - TCM	Constellation Points
V. 34 33600 TCM	TCM	Note 2	33600	3429 only	Note 2	Note 2	Note 2
V. 34 31200 TCM	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V. 34 28800 TCM	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V. 34 26400 TCM	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V. 34 24000 TCM	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V. 34 21600 TCM	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V. 34 19200 TCM	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V. 34 16800 TCM	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V. 34 14400 TCM	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V. 34 12000 TCM	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V. 34 9600 TCM	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V. 34 7200 TCM	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V. 34 4800 TCM	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V. 34 2400 TCM	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V. 23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V. 21	FSK	1080/1750	0-300	300	1	0	–
V. 17 14400 TCM	TCM	1800	14400	2400	6	1	128
V. 17 12000 TCM	TCM	1800	12000	2400	5	1	64
V. 17 9600 TCM	TCM	1800	9600	2400	4	1	32
V. 7200 TCM	TCM	1800	7200	2400	3	1	16
V. 29 9600	QAM	1700	9600	2400	4	0	16
V. 29 7200	QAM	1700	7200	2400	3	0	8
V. 29 4800	QAM	1700	4800	2400	2	0	4
V. 27 4800	DPSK	1800	4800	1600	3	0	8
V. 27 2400	DPSK	1800	2400	1200	2	0	4
V. 21 Channel 2	FSK	1750	300	300	1	0	–

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation QAM: Quadrature Amplitude Modulation
   FSK: Frequency Shift Keying DPSK: Differential Phase Shift Keying

2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	V. 34 Low Carrier	V.34 High Carrier
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

Table 2-1. MDP Pin Signals -68- Pin PLCC

Pin	Signal Label	I/O Type	Interface 3	Pin	Signal Label	I/O Type	Interface
1	NC		NC	35	RXD	OA	DTE Serial Interface
2	NC	–	–	36	VDD2	PWR	
3	NC	–	–	37	–CTS	OA	DTE Serial Interface
4	NC	–	–	38	NC	–	–
5	–RI/TXRQ	OA	DTE Serial/DMA Interface	39	NC	–	–
6	RINGD	IA	LIU: RINGD	40	DGND3	GND	–
7	–RTS	IA	DTE serial Interface	41	VDD3	PWR	–
8	IRQ	OA	Host Parallel Interface	42	NC	–	–
9	D1	IA/OB	Host Parallel Interface	43	DGND4	GND	–
10	DGND1	GND		44	NC	–	–
11	VDD1	PWR		45	NC	–	–
12	XTLI	I	Crystal/Clock Circuit	46	EYESYNC	OA	Eye Pattern Test Circuit
13	XTLO	O	Crystal/Clock Circuit	47	–EYECLK	OA	Eye Pattern Test Circuit
14	D0	IA/OB	Host Parallel Interface	48	EYEXY	OA	Eye Pattern Test Circuit
15	D2	IA/OB	Host Parallel Interface	49	NC	–	–
16	D3	IA/OB	Host Parallel Interface	50	TDCLK	OA	DTE Serial Interface
17	D5	IA/OB	Host Parallel Interface	51	–RLSD	OA	DTE Serial Interface
18	D7	IA/OB	Host Parallel Interface	52	–RDCLK	OA	DTE Serial Interface
19	DGND2	GND		53	GP0	MI	MDP: EYESYNC
20	RS0	IA	Host Parallel Interface	54	XTCLK	IA	DTE Serial Interface
21	5VA	PWR		55	DGND5	GND	
22	AGND1	GND		56	VDD4	PWR	
23	RIN	I(DA)	Line Interface	57	TXD	IA	DTE Serial Interface
24	VC	MI	To GND through capacitors	58	–DSR/RXRQ	OA	DTE Serial/DMA Interface
25	VREF	MI	To VC through capacitors	59	–RESET	OA	Host Parallel Interface
26	TXA2	O (DD)	Line Interface	60	–READ	IA	Host Parallel Interface
27	TXA1	O (DD)	Line Interface	61	–WRITE	IA	Host Parallel Interface
28	–TALK (–RLYB)	OA	Line Interface	62	–CS	IA	Host Parallel Interface
29	SPKR	O (DF)	Speaker Circuit	63	RS4	IA	Host Parallel Interface
30	AGND2	GND		64	RS3	IA	Host Parallel Interface
31	–OHRC (–RLYA)	OD	Line Interface	65	RS2	IA	Host Parallel Interface
32	–POR	MI	MDP: –RESET	66	RS1	IA	Host Parallel Interface
33	NC	–	–	67	D6	IA/OB	Host Parallel Interface
34	–DTR	IA	DTE Serial Interface	68	D4	IA/OB	Host Parallel Interface

Notes:

1. I/O types:
   - MI= Modem interconnect.
   - IA, IB= Digital input
   - OA, OB = Digital output
   - I (DA) = Analog input
   - O (DD), O (DF) = Analog output
2. NC= No external connection allowed
3. Interface Legend:
   - MDP = Modem Data Pump
   - DTE = Data Terminal Equipment

The above functions are controlled by getting an access to the interface memory in the modem through the data bus from CPU (IC27) of the control PWB. The interface memory is composed of 32 8-bit registers, and is controlled with the bank switch. Accordingly, the register is selected by the register selection signals (RS4 to RS0) of 5 bits and chip selection signal (CS). The major content controlled by these registers is as follows.

1) Configuration register

Mode setting of V34, V17, V29, V27, G2, FSK and tone transmission.

2) Option register

Equalizing method of equalizer, carrier detection threshold, addition of echo suppressor protect tone, and setting of transmission/reception mode.

3) Others

G2AGC control, tone frequency setting, and so on.

Moreover, data is read from these registers through the data bus to monitor the statuses of the modem such as tone detection, training pattern detection and so on.

Next, transmission/reception operation is described.

During sending, the sent data is given from the control block to the modem through the data bus. Then, it is modulated and sent to LIU PWB with SIGTX signal. During receiving, the received data is sent from LIU PWB to the modem with SIGRX signal and is demodulated. Then, it is sent to the control block with the data bus. The above operation is done with the modem LSI (IC).

(4) Image signal process block

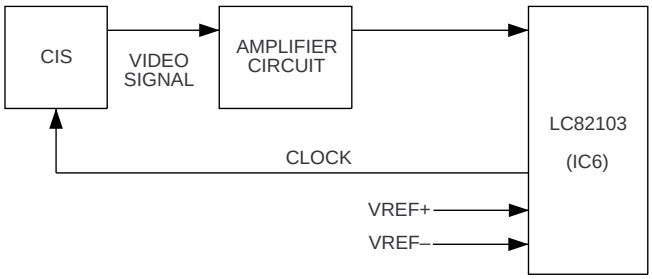


Fig. 2

The CIS is driven by the LSI (LC82103), and the output video signal from the CIS is input into the LC82103 through the amplifying circuit. The ADC and buffer are provided in the LC82103, and the digital image processing is performed.

(5) Speaker amplifier

The speaker amplifier monitors the line under the on-hook mode, outputs the buzzer sound generated from the SH7021, ringer sound, DTMF generated from the modem, and line sound.

(6) Reading process and mechanical control block

1) Mechanical control block

The mechanical control block is mainly composed of the gate array (A) (IC17: LZ9FJ59) to control the following.

(a) Sending motor control

The revolution speed and timing of the sending motor are controlled to output the control signals to the motor driver (IC7).

(b) End stamp and LED lamp control

On/off of the end stamp and LED lamp is controlled with the software.

(7) Gate array (A) block

This block is mainly composed of the gate array (A) (IC17: LZ9FJ59), and has the following functions.

① Mapper
Mapping is executed in the memory area of the memories, gate array (B), modem, CODEC and reading process LSI (LC82103).

② Mechanical control block
Refer to 1) Mechanical control block of 2-6 Reading and mechanical control block.

③ IC interface for clock
Writing and reading to IC (IC30: SM8578BV) for clock is executed in the clock-synchronous type serial transfer mode.

④ LIU control port

⑤ PC interface

- Control of PC I/F Asic (FO-47IF)

LC82103 (IC6)

Type					
I	INPUT	B	BIDIRECTION	NC	NOT CONNECT
O	OUTPUT	P	POWER		

PIN	I/O	Name	Function	PIN	I/O	Name	Function
1	B	D7	CPU interface data bus pin D7 is the MSB pin, and D0 is the LSB pin.	43	P	AVDD	Analog system power supply pin.
2	B	D6		44	I	DALRH	D/A converter high reference voltage pin for A/D converter low reference voltage.
3	B	D5					
4	B	D4		45	O	ATAPL	D/A converter monitor signal output pin for A/D converter low reference voltage.
5	B	D3					
6	B	D2		46	P	AGND	Analog system ground pin.
7	B	D1		47	B	PD7/SD	DMA output pin/serial data output pin.
8	B	D0		48	B	PD6/SDCK	DMA output pin/serial data transmission clock pin.
9	P	DGND	Digital system ground pin.				
10	P	DVDD	Digital system power supply pin.	49	P	DGND	Digital system ground pin.
11	I	A8	CPU interface address bus pin A12 is the MSB pin, and A0 is the LSB pin.	50	B	PD5/SDE	DMA output pin/serial date output valid period signal pin.
12	I	A7					
13	I	A6		51	B	PD4/PP4	DMA output pin/general-purpose I/O port pin.
14	I	A5		52	B	PD3/PP3	
15	I	A4		53	B	PD2/PP2	
16	I	A3		54	B	PD1/PP1	
17	P	DGND	Digital system ground pin.	55	B	PD0/PP0	
18	I	A2	CPU interface address bus pin.	56	P	DVDD	Digital system power supply pin.
19	I	A1		57	B	$\overline{\text{DACK}}$/PP5	DMA data acknowledge signal input pin/general-purpose I/O port pin.
20	I	A0					
21	I	$\overline{\text{WR}}$	CPU interface write signal pin.	58	B	DREQ/PP6	DMA data request signal output pin/ general-purpose I/O port pin.
22	I	$\overline{\text{RD}}$	CPU interface read signal pin.				
23	I	A12	CPU interface address bus pin.	59	B	MTP/PP7	Motor drive timing signal output pin/ general-purpose I/O port pin.
24	P	DVDD	Digital system power supply pin.				
25	I	CLKIN	System clock input pin.	60	O	CLK2	Sensor drive timing signal output pin.
26	I	A11	CPU interface address bus pin.	61	O	CLK1	
27	I	A10		62	O	RS	
28	I	A9		63	O	SH	
29	I	$\overline{\text{CS}}$	CPU interface chip select signal pin.	64	P	DGND	Digital system ground pin.
30	I	ICLK	External sampling point signal input pin.				
31	I	TRIG	External trigger signal input pin.				
32	I	$\overline{\text{RESET}}$	System reset pin.				
33	O	SAMP/LININT	A/D converter sampling point monitor signal output pin/LINE signal output pin.				
34	I	TEST	Test pin (Connect to ground in normal use.)				
35	I	$\overline{\text{REF}}$	DRAM refresh signal input pin.				
36	P	AGND	Analog system ground pin.				
37	I	DALRL	D/A converter low reference voltage pin for A/D converter low reference voltage.				
38	I	DAHRL	D/A converter low reference voltage pin for A/D converter high reference voltage.				
39	I	AIN	Sensor signal input pin.				
40	I	TEMP	Temperature signal input pin.				
41	O	ATAPH	D/A converter monitor signal output pin for A/D converter high reference voltage.				
42	I	DAHRH	D/A converter high reference voltage pin for A/D converter high reference voltage.				

Note : Not using the input pins must be connected to “Digital system power supply or ground”.

LZ9FJ59 (IC17) Terminal list

PIN	I/O	Name	Function	PIN	I/O	Name	Function
1	IO2M	RTCDT	RTC data input/output	51	IO2M	D12	System data input/output
2	O2M	RTCCK	RTC data transfer clock	52	IO2M	D11	System data input/output
3	O2M	RTCCE	RTC chip select	53	IO2M	D10	System data input/output
4	O2M	RTCIO	RTC input/output control	54	I	A7	System address input
5	TO	GAIN	Output port	55	I	A6	System address input
6	I	MTSTART	Input port	56	I	A5	System address input
7	I	LCINT	Interrupt request signal from LC82103	57	I	A4	System address input
8	O2M	XLCCS	Chip select signal to LC82103	58	I	A3	System address input
9	O	AO9	Reading/QM-coder LSI address output	59	I	A2	System address input
10	O	AO10	Reading/QM-coder LSI address output	60	IS	SHCK	Clock (19.6MHz) from CPU
11	–	GND	Ground	61	–	GND	Ground
12	O	AO11	Reading/QM-coder LSI address output	62	–	VDD	Power supply
13	O	AO12	Reading/QM-coder LSI address output	63	I	A1	System address input
14	O2M	XLCRD	Read signal to LC82103	64	I	A0	System address input
15	O2M	XLCWR	Write signal to LC82103	65	IO2M	D9	System data input/output
16	O	AO0	Reading/QM-coder LSI address output	66	IO2M	D8	System data input/output
17	O	AO1	Reading/QM-coder LSI address output	67	IO2M	D7	System data input/output
18	O	AO2	Reading/QM-coder LSI address output	68	IO2M	D6	System data input/output
19	O	AO3	Reading/QM-coder LSI address output	69	IO2M	D5	System data input/output
20	–	VDD	Power supply	70	IO2M	D4	System data input/output
21	–	GND	Ground	71	IO2M	D3	System data input/output
22	O	AO4	Reading/QM-coder LSI address output	72	IO2M	D2	System data input/output
23	O	AO5	Reading/QM-coder LSI address output	73	IO2M	D1	System data input/output
24	O	AO6	Reading/QM-coder LSI address output	74	IO2M	D0	System data input/output
25	O	AO7	Reading/QM-coder LSI address output	75	–	GND	Ground
26	O	AO8	Reading/QM-coder LSI address output	76	IS	XRESET	Reset signal
27	O	CRNT	Output port	77	O2M	XINT7	Interrupt request signal to CPU
28	–	GND	Ground	78	O2M	XINT4	Interrupt request signal to CPU
29	O	TXB1	B-phase current control output 1	79	O2M	XWAIT	Wait request signal to CPU
30	O	TXB0	B-phase current control output 0	80	I	XRAS	Input RAS signal from CPU
31	O	TXA1	A-phase current control output 1	81	I	A18	System address input
32	O	TXA0	A-phase current control output 0	82	I	A19	System address input
33	O	TXPB	B-phase current direction setting	83	I	A20	System address input
34	O	TXPA	A-phase current direction setting	84	I	A21	System address input
35	I	A12	System address input	85	I	XCS2	Chip select 2 signal input
36	I	A11	System address input	86	I	XCS6	Chip select 6 signal input
37	I	A10	System address input	87	I	XWRL	System write (high-order byte) signal
38	I	A9	System address input	88	I	XWRH	System write (low-order byte) signal
39	I	A8	System address input	89	I	XRD	System read signal
40	–	GND	Ground	90	I	XDACK0	DMA acknowledge 0 input from CPU
41	ID	QMPDRQ	DMA request input (QM-coder)	91	O2M	XDREQ0	DMA request 0 output to CPU
42	O2M	XQMPDAK	DMA acknowledge output (QM-coder)	92	I	XDACK1	DMA acknowledge 1 input from CPU
43	ID	QMCDRQ	DMA request input (QM-coder)	93	O2M	XDREQ1	DMA request 1 output to CPU
44	O2M	XQMCDAK	DMA acknowledge output (QM-coder)	94	O2M	XGABCS	Chip select (gate array B)
45	O2M	XQMRD	Read signal to QM-coder	95	O2M	XSRAMCS	Chip select (SRAM)
46	O2M	XQMWR	Write signal to QM-coder	96	O2M	XPGMCS	Chip select (ROM)
47	O2M	XQMCS	Chip select signal to QM-coder	97	I	XMDMINT	Interrupt request signal from Modem
48	IO2M	D15	System data input/output	98	O2M	XMDMCS	Chip select (Modem)
49	IO2M	D14	System data input/output	99	O	XMDMRST	Modem reset output
50	IO2M	D13	System data input/output	100	–	VDD	Power supply

LZ9FJ59 (IC17) Terminal list

PIN	I/O	Name	Function	PIN	I/O	Name	Function
101	–	GND	Ground	131	O2M	XD6004RD	Read signal to D6004 (PC I/F)
102	O2M	XEXCS	Chip select (spare)	132	O2M	XD6004WR	Write signal to D6004 (PC I/F)
103	I	XCDCINT	Interrupt request signal from CODEC	133	O2M	D6004ALE	Address strobe signal to D6004 (PC I/F)
104	I	XCDCDRQ	DMA request signal (CODEC)	134	–	GND	Ground
105	O2M	XCDCCS	Chip select (CODEC)	135	IO	AD7	PC I/F address/data input/output
106	O	XWR	System write output	136	IO	AD6	PC I/F address/data input/output
107	O2M	FLBK4	Bank control 4	137	IO	AD5	PC I/F address/data input/output
108	O2M	FLBK3	Bank control 3	138	IO	AD4	PC I/F address/data input/output
109	O2M	FLBK2	Bank control 2	139	IO	AD3	PC I/F address/data input/output
110	O2M	FLBK1	Bank control 1	140	IO	AD2	PC I/F address/data input/output
111	IU	XFLBSY	Flash memory busy signal input	141	–	GND	Ground
112	IU	FLSZ0	Input port	142	–	VDD	Power supply
113	IU	FLSZ1	Input port	143	IS	CK16M	16MHz clock input
114	O2M	XFLSTD	Chip select (flash standard)	144	ID	TEST1	Test terminal
115	O2M	XFLOPT	Chip select (flash option)	145	IO	AD1	PC I/F address/data input/output
116	IU	XCI	Input port	146	IO	AD0	PC I/F address/data input/output
117	IU	XRHS	Input port	147	IU	XB4FRS	Input port
118	IU	XEXHS	Input port	148	IU	XFRSNS	Input port
119	TO	DPON	Output port	149	IU	XORGSNS	Input port
120	–	GND	Ground	150	IU	XROLSNS	Input port
121	TO	TXMUTE	Output port	151	I	PRTSNS1	Input port
122	IU	HSDTCT	Input port	152	TO	CDCMSK	Output port
123	TO	MPXC	Output port	153	TO	PLG0ON	Plunger 0 control
124	TO	MPXB	Output port	154	TO	PLG1ON	Plunger 1 control
125	TO	DPMUTE	Output port	155	TO	LEDON	CIS LED light source control
126	IU	PCDTCT	Input port	156	IU	XEXINT0	Interrupt request signal from PC I/F
127	TO	FAXPCSL	Output port	157	IU	XEXINT1	Interrupt request signal (spare)
128	O2M	XD9001CS	Chip select (PC I/F D9001)	158	I	PCIFSL	PC I/F select signal input
129	O2M	XD9001RW	Read signal to D9001 (PC I/F)	159	IO2M	IOP0	Input port (spare)
130	O2M	XD9001WR	Write signal to D9001 (PC I/F)	160	–	GND	Ground

I : Input terminal (TTL level input)
IS : Input terminal (TTL level schmitt input)
IU : Input terminal (TTL level input, pull up resistor 250 KΩ building in)
ID : Input terminal (TTL level input, pull down resistor 250 KΩ building in)
IO : Input/output terminal (TTL level input, output electric current: I_{OL}=4.0 mA)
IO2M : Input/output terminal (TTL level input, output electric current : I_{OL}=2.0 mA)
O : Output terminal (Output electric current: I_{OL}=4.0 mA)
O2M : Output terminal (Output electric current: I_{OL}=2.0 mA)
TO : Try-state output terminal (Output electric current: I_{OL}=4.0 mA)
VDD : Power supply
GND : Ground

(8) Gate array (B) block

The block is composed of the gate array (B) and SRAM (2 KByte).

1) LR38292(IC10) ... pin-160, QFP (gate array B)

The device has the following functions.

① Printing data process
The image data of the page memory for printing is converted into 400 dpi, and the smoothing and contracting processes are applied.

② Printer (PCU) interface
The control of resetting and so on to PCU and the image data processed in Item ① above are synchronized with the signal (HSYNC) from PCU and are transmitted to PCU in the serial mode.

③ DMA controller
(a) The binary-coded data of the draft transmitted in the serial mode from the gate array (A) LZ9FJ59(IC17) and read with the scanner are transmitted to the page memory.
(b) The image data which will be printed are read from the page memory, and the process ① is applied to transmit the data to PCU in the serial mode.

④ CODEC (HD813201F) interface
(a) The timing is controlled for CPU to get an access to CODEC.
(b) The timing is controlled for CODEC to get an access to the page memory.

⑤ DRAM controller
Since DRAM is used for the page memory, and the address, RAS and CAS are controlled and refresh-controlled.

⑥ Panel interface
The key input detection on the operation panel, LED lighting control and LCD display control are executed.

2) LH5116NA-10 (IC3) -- pin-24, SOP (16-Kbit SRAM)

This SRAM is a line memory for the printing data process (resolution power conversion, smoothing and contracting to 404 dpi) of the gate array (B).

LR38292 (IC10) Terminal descriptions

Pin	Name	I/O	Function
20	VCC		Power supply
62	VCC		
100	VCC		
142	VCC		
16	GND		Ground
21	GND		
35	GND		
48	GND		
61	GND		
78	GND		
87	GND		
101	GND		
125	GND		
134	GND		
143	GND		
65	MANRESB	O	Manual reset signal
66	RESETB	I	Reset signal
89	A5	I	Address signal on the system side
90	A4		
91	A3		
92	A2		
93	A1		
70	D15	I/O	Data bus signal on the system side
71	D14		
72	D13		
73	D12		
74	D11		
75	D10		
76	D9		
77	D8		
79	D7		
80	D6		
81	D5		
82	D4		
83	D3		
84	D2		
85	D1		
86	D0		
88	CSB	I	Chip select signal of gate array LR38292
97	RDB	I	Read signal on the system bus side
98	WRB	I	Write signal on the system bus side
115	SHCK0B	O	Reversion output of clock (SHCK) from CPU
116	SHCK	I	Clock (19.6 MHz) from CPU
95	GAINTB	O	Interrupt request signal to CPU of gate array LR38292
94	CDCINTB	O	Reversion output (to CPU) of interrupt request signal from HD813201F
96	DREQ0B	O	Reversion output (to CPU) of DMA transfer request signal from HD813201F
99	RSTCDCB	O	Reset signal to HD813201F (Default: Low)
102	CDCINT	I	Interrupt request signal from HD813201F
103	BRQT	I	Bus right request signal of image bus from HD813201F
104	BACKB	O	Bus right permission signal of image bus to HD813201F
105	DRQ0	I	DMA transfer request signal from HD813201F
106	DACK0B	O	Acknowledge signal of DMA transfer to HD813201F
107	CSCDCB	I	Chip select signal to HD813201F
108	MDENB	I	Data enable signal of image bus from HD813201F
109	READY	O	Ready signal of image bus access to HD813201F
110	MAS	I	Address strobe signal of image bus of HD813201F

LR38292 (IC10) Terminal descriptions

Pin	Name	I/O	Function
111	MAENB	I	Address enable signal of image bus of HD813201F
112	CK16M	I	16 MHz clock input
113	RDCDC	O	Register read signal (active H) of HD813201F of CPU
114	RDCDCB	O	Register read signal (active L) of HD813201F of CPU
139	MA20	I	Address of image bus of HD813201F
138	MA19		
137	MA18		
136	MA17		
135	MA16		
133	MAD15	I/O	Address/data of image bus of HD813201F Input mode is selected when HD813201F gets an access to image bus (MAENB=L). Data bus to memory (page memory) is selected when gate array LR38292 gets an access to the image bus.
132	MAD14		
131	MAD13		
130	MAD12		
129	MAD11		
128	MAD10		
127	MAD9		
126	MAD8		
124	MAD7		
123	MAD6		
122	MAD5		
121	MAD4		
120	MAD3		
119	MAD2		
118	MAD1		
117	MAD0		
155	DA11	I/O	Address bus to memory of image bus (page memory) When HD813201F gets an access to the image bus, address of MA21 thru MA16, MAD15 thru MAD1 are converted to Row/Column address in the page memory (DRAM) and output. When gate array LR38292 gets an access to the image bus, Row/Column address is output to the page memory (DRAM).
154	DA10		
153	DA9		
152	DA8		
151	DA7		
150	DA6		
149	DA5		
148	DA4		
147	DA3		
146	DA2		
145	DA1		
144	DA0		
156	DWEB	O	Write signal to memory (page memory: DRAM) of image bus
157	RAS1B	O	RAS1 signal to memory (page memory: DRAM) of image bus
158	RAS0B	O	RAS0 signal to memory (page memory: DRAM) of image bus
159	CASB	O	CAS signal to memory (page memory: DRAM) of image bus
140	DRMSIZE	I	Setting of size of memory (page memory: DRAM) of image bus Low: 16 Mbits High: 12 Mbits
141	DRMTYPE	I	Setting of type of memory (page memory: DRAM) of image bus Low: Address 8-bit type High: address 12-bit type (Valid only for DRMSIZE=L. Don't care for DRMSIZE=H.)
67	STVDB	I	Serial scanner data valid range signal
68	SRVID	I	Serial scanner data
69	SCCLK	I	Serial scanner data transfer clock
51	PCURESB	O	Reset signal for printer unit
52	HSYNC	I	Main scanning synchronous signal from printer unit
53	EPRDYB	I	Communication ready signal from printer unit
54	PRRDYB	I	Printing operation ready signal of printer unit
55	TODB	I	Sub-scanning synchronous signal to printer unit

Pin	Name	I/O	Function
56	ETBSYB	I	Status sending signal of printer unit
57	CTBSYB	O	Command sending signal to printer unit
58	PRINTB	O	Printing start/continuation signal to printer unit
59	PDATA	O	Printing image data to printer unit
60	CPRDYB	O	Communication ready signal to printer unit
63	XIN	I	Clock input (quartz oscillator connection)
64	XOUT	O	Clock output (quartz oscillator connection)
38	LMA10	O	Address bus of line memory for smoothing/contracting
37	LMA9		
36	LMA8		
34	LMA7		
33	LMA6		
32	LMA5		
31	LMA4		
30	LMA3		
29	LMA2		
28	LMA1		
27	LMA0		
40	LMD7	O	Data bus of line memory for smoothing/contracting
41	LMD6		
42	LMD5		
43	LMD4		
44	LMD3		
45	LMD2		
46	LMD1		
47	LMD0		
39	LMWEB		
26	LD15	I/O	Control/data bus and LED on/off control signal to key scan and LCD driver on the operation panel
25	LD14		
24	LD13		
23	LD12		
22	LD11		
19	LD10		
18	LD9		
17	LD8		
15	LD7		
14	LD6		
13	LD5		
12	LD4		
11	LD3		
10	LD2		
9	LD1		
8	LD0		
160	SEN7	I	Key input detection signal of operation panel
1	SEN6		
2	SEN5		
3	SEN4		
4	SEN3		
5	SEN2		
6	SEN1		
7	SEN0		
49	MEMTST	I	Terminal for device test of integrated memory Low is set except in the device test mode.
50	TEST	I	Terminal for device test Low is set except in the device test mode.

(9) CODEC block

This block is composed of CODEC, LS374 and LS244 in order to demodulate the contracted image data of the draft read with the scanner and the letter image transmitted in the DMA mode from the system memory.

1) HD813201F (IC12) ... pin-80, 6FP (CODEC)

It operates at 16 MHz corresponding to the crystal oscillator (X2) of 16 MHz.

The image memory is commonly used as the page memory. The image data of the draft read with the scanner in the page memory is contracted by MMR, and is transferred to the system memory (DRAM: IC16) by the DMA transfer function of CPU. Moreover, the image data transferred in the DMA mode from the system memory are demodulated with MMR, and are developed into the page memory.

2) HD74LS374 (IC18) ... pin-20, SOP

The data hold time during writing from main CPU to HD813201F is assured.

3) HD74LS244 (IC20) ... pin-20, SOP

When the main CPU reads the inner register of HD813201F, it will read the data through this buffer.

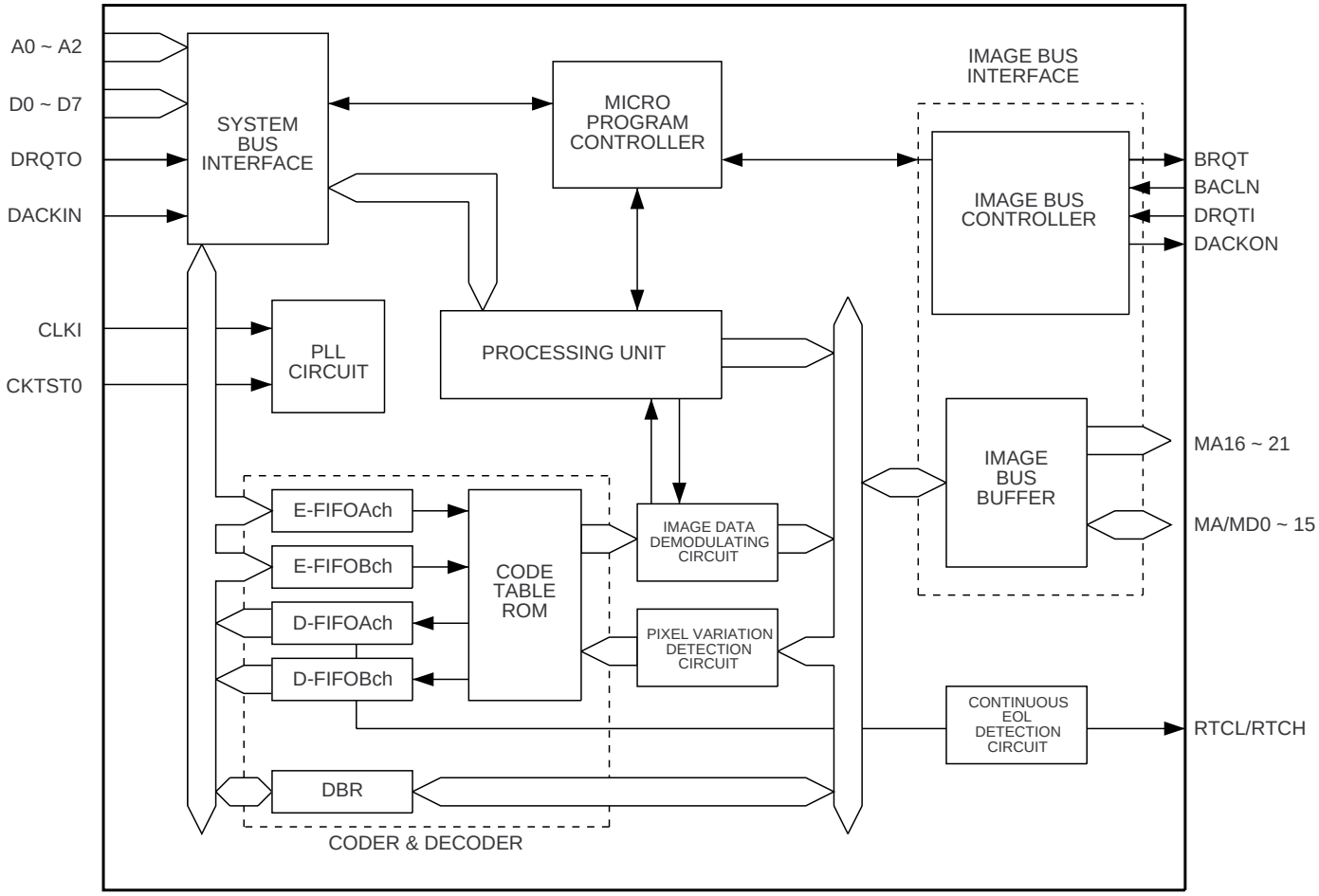


Fig. 3

HD813201F (IC12) Terminal descriptions

Code	Terminal No.	I/O	Function
$\overline{68}$/80	56	I	If this terminal is at "low" level, it indicates that MPU of system 88 is connected to IDP201. "High" level indicates that MPU of system 80 is connected.
A0	57	I	Addresses 0 thru 2 (address terminals). It is connected to the low-order 3 bits of the system address bus, and MPU is used to get an access to the internal register of IDP201.
A1	54		
A2	55		
D0	64	I/O, Three-state output	Data 0 thru 7 (data terminals). They are connected to the system data bus for bidirectional data transfer between MPU and IDP201. MPU can read and write the internal register of IDP201.
D1	62		
D2	65		
D3	63		
D4	67		
D5	66		
D6	68		
D7	69		
$\overline{CS}$	44	I	Chip select (chip select terminal). When the terminal is at "low" level, it indicates that MPU gets an access to the internal register of IDP201.
DS	45	I	Data strobe (data strobe terminal). Connect ϕ2 clock pin of MPU of system 88 or $\overline{RD}$ pin of MPU of system 80.
R/$\overline{W}$	42	I	Read/write (read/write terminal). Connect R/$\overline{W}$ pin of MPU of system 88 or $\overline{WR}$ pin of MPU of system 80.
$\overline{RESET}$	59	I	Reset element. If the signal of "low" level is input to the terminal, IDP201 will be initialized.
IRQT	58	O	Interrupt request (interrupt request terminal). When the signal of "high" level is output, IDP201 requests the interrupt process for MPU. The factor of the interrupt is the end of the command process, the end of DMA transfer, occurrence of an error during demodulation or the receiving of RTC code. MPU reads IRR (interrupt request register) which is one of the internal registers of IDP201, and can know the factor of the interrupt. When MPU reads IRR, IRQT becomes "low" level. (For details of IRR, refer to "8.1.2 Interrupt request register".)
DRQTO	47	O	DMA Request Output (DMA request output terminal). In the following cases, DMA transfer can be requested for DMAC by turning DRQTO to "high". (1) During coding, a code of 1 byte or more is stored in E-FIFO. (2) During decoding, an empty area of 1 byte or more is present. (3) During data transfer between the system bus and image bus, DBR is read to read or write.
$\overline{DACKI}$	46	I	DMA Acknowledge Input (DMA acknowledge input terminal) The response signal for DRQTO is input. If $\overline{DACKI}$ becomes "low" level during coding or decoding, the access is given to E-FIFO or D-FIFO. If $\overline{DACKI}$ becomes "low" level during data transfer between system bus and image bus, the access is given to DBR. Don't make $\overline{CS}$ and $\overline{DACKI}$ "low" at the same time.
BRQT	52	O	Bus Request (Bus request terminal). IDP201 outputs the signal of "high" level from BRQT, and IDP201 requests the bus master for the device which can become another bus master on the image bus. If any other device which can become the bus master on the image bus, BRQT becomes the NC pin.
$\overline{BACK}$	48	I	Bus Acknowledge (bus acknowledge terminal). The response signal for BRQT is input. If the signal of "low" level is input to $\overline{BACK}$, it indicates that it is approved for IDP201 to become the bus master of the image bus. If any other bus master which can become the bus master is not present except IDP201, fix this terminal at "low".
$\overline{MAEN}$	76	O	Memory Address Enable (Memory address enable terminal). IDP201 outputs the signal of "low" level from $\overline{MAEN}$ to declare that it becomes the bus master of the image bus. When $\overline{MAEN}$ is at "high", the three-state output which is connected to the image bus becomes all into the high impedance state.

HD813201F (IC12) Terminal descriptions

Code	Terminal No.	I/O	Function
MAS	74	O	Memory Address Strobe (Memory address strobe terminal). When MAS becomes "high" level, it indicates that address is output to MA/MD0 thru MA/MD15 and MA16 thru MA21.
UDS	27	Three-state output	Upper Data Strobe (high-order data strobe terminal). When $\overline{UDS}$ becomes "low" level, it indicates that IDP201 uses the high-order byte of the image bus.
$\overline{LDS}$	23	Three-state output	Upper Data Strobe (low-order data strobe terminal). When $\overline{LDS}$ becomes "low" level, it indicates that IDP201 uses the low-order byte of the image bus.
$\overline{MDEN}$	25	O	Memory Data Bus Enable (Memory data bus enable terminal). When $\overline{MDEN}$ output terminal becomes "low" level, it indicates that valid data are present in MA/MD0 thru MA/MD15. This output terminal is used to control the output of the bidirectional bus buffer on MA/MD0 thru MA/MD15.
MA/MD 0	79	I/O, Three-state output	Memory Address Data Bus 0 thru 15 (Memory address data bus). In this bus for image bus operation, the address and data are multiplexed. MA/MD0 thru MA/MD15 are used as follows. (1) When $\overline{MAEN}$ is "low" and MAS is "high", it is used as the output address line. (2) When both $\overline{MAEN}$ and $\overline{MDEN}$ are "low" in the reading cycle, it is used as the input data line. (3) When both $\overline{MAEN}$ and $\overline{MDEN}$ are "low" in the writing cycle, it is used as the input data line.
MA/MD 1	77		
MA/MD 2	3		
MA/MD 3	78		
MA/MD 4	5		
MA/MD 5	2		
MA/MD 6	6		
MA/MD 7	4		
MA/MD 8	8		
MA/MD 9	7		
MA/MD10	12		
MA/MD11	9		
MA/MD12	14		
MA/MD13	13		
MA/MD14	15		
MA/MD15	16		
MA16	71	Three-state output	Memory Address Bus 16 thru 21 (memory address bus). When $\overline{MAEN}$ is "low" and MAS is "high", it is used as the output address line.
MA17	11		
MA18	30		
MA19	31		
MA20	50		
MA21	51		
$\overline{MR}$	26	Three-state output	Memory Read (Memory read terminal). When $\overline{MR}$ is turned to "low" level, IDP201 reads the data from the image memory.
$\overline{MW}$	28	Three-state output	Memory Write (memory write terminal). When $\overline{MW}$ is turned to "low" level, IDP201 writes the data in the image memory.
$\overline{IOR}$	35	Three-state output	I/O Read (I/O read terminal). When $\overline{IOR}$ is turned to "low" level, IDP201 reads the data from I/O device on the image bus. However, it is limited at DMA transfer during data transfer with the transfer command and the coding process.
$\overline{IOW}$	36	Three-state output	I/O Write (I/O write terminal). When $\overline{IOW}$ is turned to "low" level, IDP201 writes the data in I/O device on the image bus. However, it is limited at DMA transfer during data transfer with the transfer command and the decoding process.
DRQTI	39	I	DMA Request Input (DMA request input terminal). When I/O device on the image bus requests DMA for IDP201, DRQTI becomes "high" level.
$\overline{DACKO}$	38	O	DMA Acknowledge Output (DMA acknowledge output terminal). When this output terminal is turned to "low" level, IDP201 informs to the peripheral devices on the image bus that DMA operation is approved.
$\overline{DMA}$	32	O	Direct Memory Access (Direct memory access terminal). When $\overline{DMA}$ output is turned to "low", it indicates that DMA transfer is executed. In the coding process, the data is transferred from the I/O device (scanner) to the image memory. In the decoding process, the data is transferred from the image memory to I/O device (printer).

HD813201F (IC12) Terminal descriptions

Code	Terminal No.	I/O	Function
DTC	37	O	DMA Terminal Count (DMA terminal count terminal). When DTC output is turned to "high", it indicates that DMA transfer of the setting line part is ended.
READY	73	I	Image memory or I/O device read. When READY is turned to "high" during writing, it indicates that the image memory or I/O device is ready for transmitting/receiving the data. When READY is "high", IDP201 will wait until READY becomes "high".
<Power terminal>			
V_{DD} 1	29	I	Power voltage (+5V)
V_{DD} 2	49	I	
V_{DD} 3	72	I	
V_{SS} 1	10	I	
V_{SS} 2	17	I	Ground
V_{SS} 3	34	I	
V_{SS} 4	53	I	
V_{SS} 5	70	I	
V_{SS} 6	75	I	
<Other>			
TEST 0	18	I	Fix these terminals at "low".
TEST 1	22	I	
TEST 2	24	I	
TEST 3	33	I	
TEST 4	43	I	

Code	Terminal No.	I/O	Name and function
CLKI	19	I	Quartz oscillation input terminal and external clock input terminal.
CLKX	20	O	Quartz oscillation output terminal.
CKTST1	1	I	Low pass filter terminal of PLL circuit. Connected to capacitor (1000pF) and resistor (10kΩ) through GND.
CLKMOD	40	I	Terminal to switch quartz oscillation connection or external clock input mode. "0": Quartz oscillation. "1": External clock.
CKTST0	41	I	Fix at "LOW" level.
CLKO	21	O	Clock output terminal. Rectangular wave which is synchronous with the internal clock of IDP201 is output.
CKTST2	80	I	Fix at "LOW" level.

Code	Terminal No.	I/O	Name and function
RTCH	60	O	Number of transfers of EOL detected by IDP201 during RTC receiving is reflected at the terminal.
RTCL	61	O	

(10) Page memory block

The page memory block is composed of one DRAM of 1M × 16 bits, being commonly used as the image memory. The memory is divided into the page memory for the scanner and the page memory for printing.

The page memory for scanner is composed of the partial area of IC9. The image data of approx. one page (except in the super fine mode) of the draft read with the scanner can be stored. They are stored until they are contracted by CODEC.

The page memory for printing is composed of the remaining areas of IC9 and can store approx. one page of the image data decoded by CODEC. The data are stored until they are transferred to PCU with the gate array (B) and printed.

(11) Driver block

Sending motor driver (IC7: LB1845) ---- 28-pin DIP
This IC driver at the sending motor at the constant current with the bipolar, chopper system.

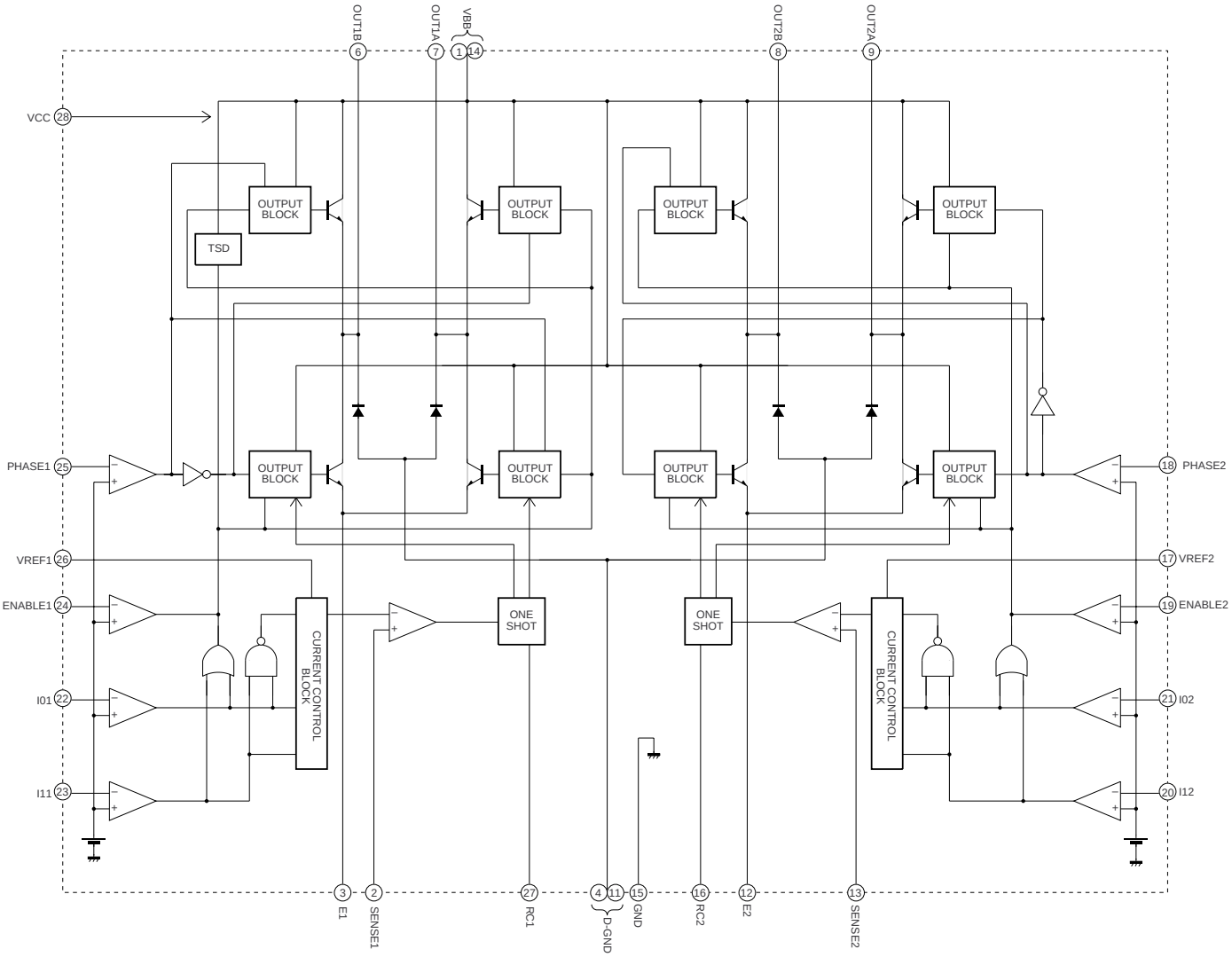


Fig. 4

[Truth Table]

ENABLE	PHASE	OUTA	OUTB
L	H	H	L
L	L	L	H
H	–	OFF	OFF

I_0	I_1	Output Current
L	L	Vref/ (10 x R_E) = I_{OUT}
H	L	Vref/ (15 x R_E) = I_{OUT} x 2/3
L	H	Vref/ (30 x R_E) = I_{OUT} x 1/3
H	H	0

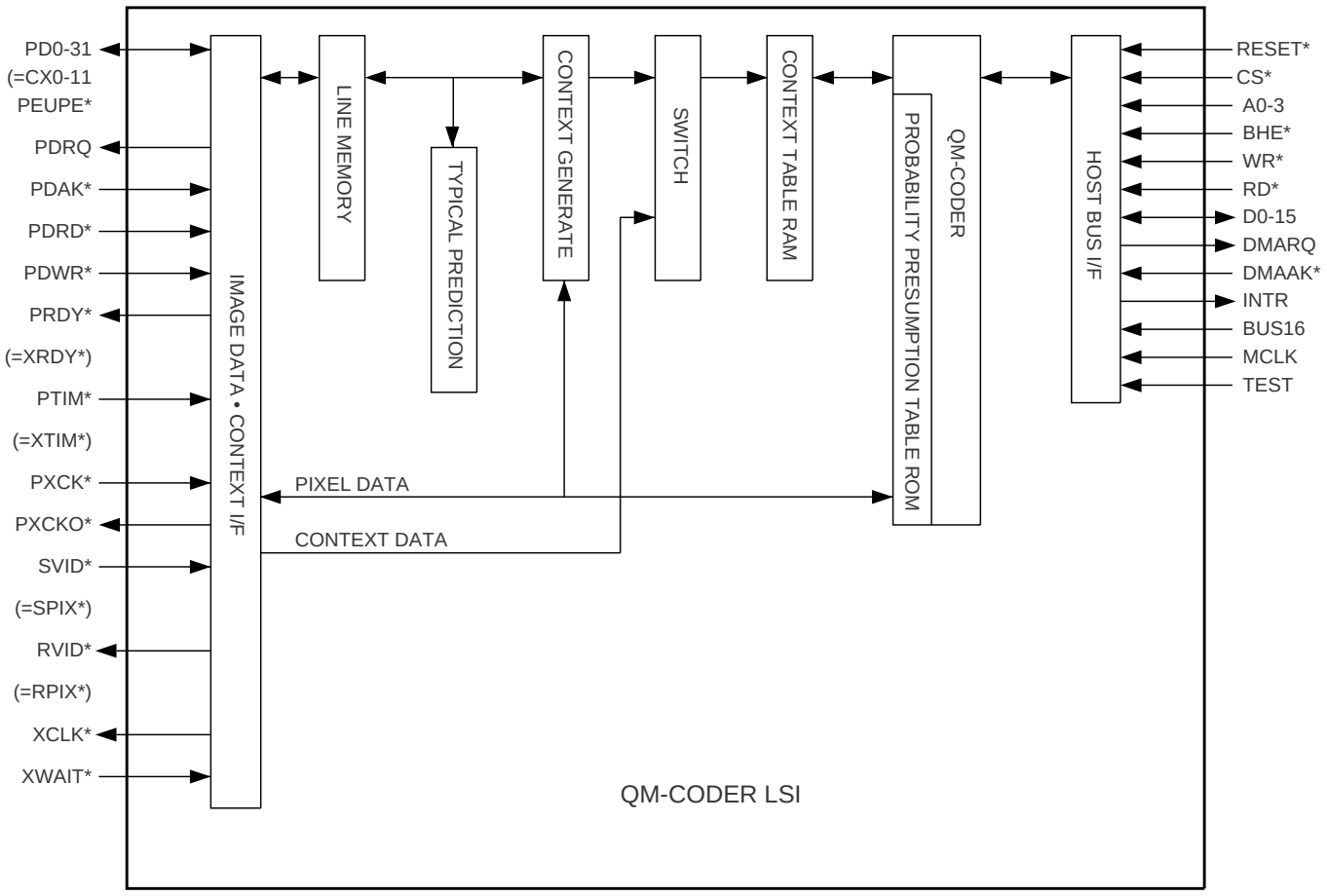
Note: When ENABLE = H or I_0 = I_1 = H, the output is in OFF state.

[Pin Functions]

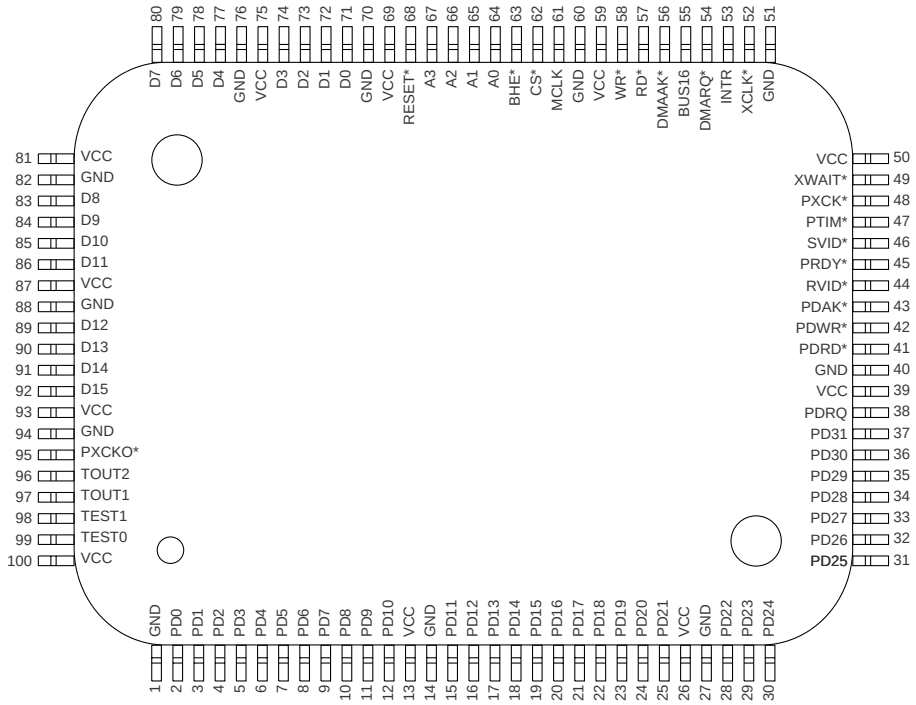
Pin name	Pin No.	Pin Description
VBB	1, 14	Output stage power-supply voltage
SENSE1 SENSE2	2 13	Set current detection pins. Connect these pins, fed back through noise filters, to E1, and E2.
E1 E2	3 12	Current control pins by connecting between this pin and GND.
DGND	4,11	Internal diode anode connection
OUT1B OUT1A OUT2B OUT2A	6 7 8 9	Output pins
GND	15	Ground
RC1 RC2	27 16	Used to set the output off time for the switched output signals. The fixed off times are set by the capacitors and resistors connected to these pins. t off ≒ CR
Vref1 Vref2	26 17	Output current settings The output current is determined by the voltage (in the range 1.5 to 7.5V) input to these pins.
PHASE1 PHASE2	25 18	Output phase switching inputs. [H] input : OUT A = high, OUT B = low [L] input : OUT A = low, OUT B = high
ENABLE1 ENABLE2	24 19	Output on/off settings [H] input : output OFF [L] input : output ON
I01, I11 I02, I12	22, 23 21, 20	Digital inputs that set the output current The output currents can be set to 1/3, 2/3, or full by setting these pins to appropriate combinations of high and low levels.
VCC	28	Logic block power supply.

(12) JBIG block

When it sends FAX by the JBIG compression form, the JBIG compression of the image data and JBIG expansion are done with QM-CODER LSI of IC23 (M65761).



IC23: VHiM65761FP-1(M65761FP)



M65761FP (IC23) Terminal descriptions

I/F	Signal name	Terminal No	I/O	Function	
Host bus I/F (29 pin)	RESET*	68	I	H/W reset signal.	
	CS*	62	I	Chip select signal.	
	A0-3	64,65,66,67	I	Address select signal of inner register.	
	BHE*	63	I	Access signal of upward byte (D8-15).	
	WR*	58	I	Write strobe signal.	
	RD*	57	I	Read strobe signal.	
	D0-15	71~74, 77~80, 83~86, 89~92	IO	Input/output data signal. (Use D0-7 when 8 bit bus)	
	DMARQ	54	O	DMA request signal of encode data.	
	DMAAK*	56	I	DMA acknowledge signal of encode data.	
	INTR	53	O	Interrupt request signal.	
	BUS16	55	I	8 bit bus (D0-7) and 16 bit bus (D0-15) function select line.	
Image data I/F Parallel	PD0-31	2~12 15~25 28~37	IO	Parallel image input/output bus. (Use PD0-15 when 16 bit bus)	
	PDRQ	38	O	DMA request signal of image data.	
	PDAK*	43	I	DMA acknowledge signal of image data.	
	PDRD*	41	I	Read strobe signal of image data.	
	PDWR*	42	I	Write strobe signal of image data.	
Image data I/F Serial	PRDY*	45	O	1 line input/output start ready signal of image data.	
	PTIM*	47	I	1 line transfer section signal of image data.	
	PXCK*	48	I	Transfer clock signal of image data.	
	PXCKO*	95	O	Transfer synchronization clock signal of image data.	
	SVID*	46	I	Input signal of image data.	
	RVID*	44	O	Output signal of image data.	
Context I/F	CX0-11	2~12,15	I	Context input. (CX0 is possible to feed back in LSI)	(=PD0-11)
	PEUPE*	19	I	Updata enable of RAM for PE. (Learning function ON/OFF)	(=PD15)
	SPIX*	46	I	Encode image data input signal.	(=SVID*)
	RPIX*	44	O	Decode image data output signal.	(=RVID*)
	XCLK*	52	O	Context data transfer clock signal.	
	XWAIT*	49	I	Context data transfer wait signal.	
	XRDY*	45	O	Context data 1 stripe input/output start ready signal.	(=PRDY*)
	XTIM*	47	I	Context data 1 stripe transfer section signal.	(=PTIM*)
Others	MCLK	61	I	Master clock input signal.	
	TEST0-1	98,99	I	Signal for test. (Usually connect to GND)	
	VCC/GND	1,13,14,26,27, 39,40,50,51,59, 60,69,70,75,76, 81,82,87,88,93, 94,100	–	Power(+5V)/Ground.	

Note : Most of context IF signal line is shared with image data I/F signal line.
It is shown that * of the signal name is negative logic.

[2-1] Circuit description of memory PWB

It is composed by the flash memory of 2Mbyte, and attached to the CNOP connecter of the control PWB circuit. It can be expanded by substituting FO-3MK(OPTION) for the standard memory PWB to 5MB.

1) LH28F016SUT(IC4) ... pin-56, TSOP (16 Mbit flash memory)

This memory is a nonvolatile type whose content does not volatilize even if power is turned off, and stores the copied, sent and received image data. Moreover, the initially registered data, registered content of “RELAY” key and registered content of “CONF” key are stored.

2) W24010S-70L(IC21, IC36) ... pin-32, SOP (1 Mbit SRAM)

The setting of receiving mode, optional setting content, soft switch content and daily data are stored. Even if the power supply of the main body is turned off, it is backed up with a lithium battery.

[2-2] Circuit description of 3rd. cassette PWB

1. Circuit system

A clock pulse of 1000Hz is sent from the mechanism computer CPU (pin 17 of IC2) and a motor driving pulse signal of 500 PPS is generated at the shift register HC 164.
The driving motor for the 3rd. cassette is driven with two-phase excitation by a driving pulse (the output pulse from the HC164) using the low voltage drive system of 24V.